METHOD AND APPARATUS FOR FRACTIONAL RF SIGNAL SYNTHESIS

This application Claims priority under 35 U.S.C. 119 from Provisional Application Serial No. 60/511,677 filed October 17th 2003.

This invention relates generally to telecommunication systems. The present invention relates more specifically to a method of synthesizing an RF signal used in telecommunication systems.

This application is related to applications filed on the same day by the same inventors under Attorney Docket 85195-502 ADB entitled APPARATUS FOR DIGITAL VECTOR QAM MODULATOR and Attorney Docket 85195-602 ADB entitled APPARATUS FOR FRACTIONAL RF SIGNAL SYNTHESIS WITH PHASE MODULATION the disclosures of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

In communication systems an oscillator is used as a fundamental building block. Oscillators are commonly used for up and down frequency conversion. They are also required for subsystems such as a direct modulator. The quality of a fixed frequency oscillator is measured by the frequency accuracy and the phase noise performance. In communication systems, the basic RF oscillator is used in conjunction with additional circuitry to stabilize the frequency of the oscillator as typical free running RF oscillators are not stable enough for most communication systems. It is well known that crystal oscillators provide a high degree of frequency accuracy and phase noise performance. Hence, it is common in prior art to lock the RF oscillator to a lower frequency crystal oscillator in order to achieve the desired frequency stability. Besides frequency stability, other qualities including the ability to

tune a single oscillator over a wide frequency range, the ability of having a very fine frequency resolution control, and the ability to change the frequency very rapidly are quite imperative.   Numerous prior art methods exist for the generation of an oscillator subsystem with varying degrees of compromises and limitations.

5   Commonly used methods are discussed below and are described in more detail hereinafter in conjunction with the accompanying drawings. .

The first method uses frequency multiplication wherein crystal oscillators that are commonly available at low frequencies are multiplied up using frequency multiplication.   This method yields a high phase noise performance but

10   suffers from very limited frequency agility.

The second method uses a phase locked loop (PLL).   PLLs are available in a variety of forms such as fixed modulus, dual modulus, and fractional N. Many integrated circuit implementations are available.   However a PLL with lower loop bandwidth thus has to be used which consequently degrades the phase noise.

15   The third method is a digital delay lock loop (DLL).   This has the advantage that the oscillator is suitable for implementation in an ASIC. A variable delay control is used in conjunction with the phase detector to lock the oscillator frequency to a multiple of the input reference frequency. This method suffers from limitations to the PLL implementation. It also faces additional problems with

20   frequency agility as well as the jitter introduced by the delay lock loop because of mismatched delays.

The fourth method is known as direct digital synthesis (DDS).   This method results in very fine frequency resolution, but produces undesired spurious

signals and the output signal frequency is limited by the speed of the DAC. The signal frequency for the DDS is limited to Nyquist frequency which is half of the clock frequency to the DAC. Output signal level drops as the Nyquist frequency is approached.

5   A fifth method is through phase interpolation as described in patent number 6,114,914 (Mar) issued September 5th 2000. This method is limited in its factional capability and still uses a VCO, phase detector, and loop filter. Normal conflict between better phase noise and higher frequency resolution still exists for this method.

10   SUMMARY OF THE INVENTION

According to the present invention there is provided an apparatus for direct digital generation of a synthesized RF signal at a desired output frequency comprising:

a high speed reference clock providing in an input signal having a

15   series of signal reference edges at a frequency of the reference clock which is higher than the desired output frequency;

programmable digital delay elements arranged to receive the reference edges of the input reference clock and to generate delayed signal edges each at a calculated delay from a respective reference edge;

20   and a signal combining element for receiving the delayed signal edges and for generating the RF signal therefrom.

Preferably the output frequency is set from an increment value according to the following equation:

Increment Value = $((f_{ref} / f_{out}) -1) * 2^n$

where f_{ref} = Reference clock (103) frequency

f_{out} = Output (110) frequency

n = Number of bits in the accumulator math.

5   Preferably the duty cycle is set by initializing the difference of the

initializing values of the two accumulators according to the following equation:

The reference clock frequency divided by the desired output frequency

multiplied by $2^{\wedge n}$ multiplied by (p/100), where p is the percentage duty cycle and n is

the number of bits in the accumulator math.

10   Preferably the worst case frequency resolution is determined by the

equation:

The reference frequency divided by $2^{\wedge n}$, where n is equal to the

number of bits in the accumulator.

Preferably the duty cycle of the output can be varied by changing the

15   difference in the start values of the accumulators for the rising and falling edge delay

control.

Preferably phase delay of the programmable delay is calibrated from

the phase accumulator value using a look up table or Microprocessor.

Preferably separate delay controls are used for producing the rising

20   and falling edges of the output from the same input edge of the reference clock.

Preferably the reference edge of the reference clock is delayed by the

programmable delay lines.

Preferably the reference edge may be either the rising or falling edge

of the reference clock.

Preferably the carry bits (overflow bits) are used to control a pulse swallowing circuit to extend the delay to multi cycles of the input reference clock.

Preferably the clock swallow circuit can ignore/block multiple reference clock pulses thus giving the delay line endless delay capability.

Preferably the clock swallow circuit can be located prior to or following the programmable delay line.

Preferably a set reset flipflop is used to combine the separate rising and falling edge delays to form any desired duty cycle output.

Preferably the output duty cycle is not dependent on the input duty cycle.

Preferably increasing the number of bits in the adder math increases the frequency resolution with negligible degradation in the phase noise performance.

Preferably the number of bits of math used in the adder is equal to or greater than the number of bits of control in the lookup table and /or the programmable delay.

Preferably the speed is increased using parallel processing in the adders, and/or accumulators.

Preferably the adders/accumulators is implemented in a larger lookup table wherein all the answers of the pattern are precomputed and stored.

Preferably an optional arrangement could include plurality of adders, accumulators, pulse swallow circuits, lookup tables, and programmable delay lines.

Preferably the lookup table has a multiple set of lookup tables to be

used for temperature compensation of the programmable delay line.

Preferably the implementation is done fully digitally in an ASIC with no requirement for a voltage controlled oscillator, loop filter, or Digital to Analog converter used in prior art solutions.

5   Preferably an optional arrangement could include amplification and filtering of the output to produce a signal that is higher in amplitude and/or having less harmonics.

It is an object of the present invention to provide an RF signal that has superior phase noise and frequency resolution with the additional benefits of 10   instantaneous frequency change capability, wide frequency range ability, and suitability for digital ASIC implementation with no external components.

The present invention is based on digital generation of an RF signal from a higher frequency reference signal using pulse stretching to delay each edge of the reference clock to the desired time instant. In the proposed method, provision 15   is made to swallow a clock edge when required thereby allowing the synthesis of any desired lower frequency from DC to the reference input frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a Prior Art Frequency Multiplier.

Figure 2 is a block diagram of a Prior Art Phase Locked Loop (PLL).

20   Figure 3 is a block diagram of a Prior Art Digital Delay Locked Loop (DLL).

Figure 4 is a block diagram of a Prior Art Direct Digital Synthesis (DDS).

Figure 5. is a block diagram of a System for RF signal synthesis.

Figure 6 is a Timing diagram for Sample shown in Table 1.

Table 1 is a Sample timing calculations for Invention

DETAILED DESCRIPTION

5   Figure 1 illustrates the first method mentioned above where a crystal oscillator 10 is subjected to a nonlinearity in order to realize a frequency multiplier 11. The desired multiplied frequency is filtered using a band pass filter 12, resulting in the RF output frequency 13. This method yields a high phase noise performance but suffers from very limited frequency agility.

10   The basic principal of a PLL as mentioned in the second method above is shown in Figure 2. As illustrated in the figure, a stable reference frequency 20 is divided down 21. The output RF signal frequency 26 is also divided down 25. The two divided frequency signals are then fed to the phase detector 22 for phase comparison. The phase detector 22 is used to produce an error signal that is filtered

15   23 with the required loop bandwidth to lock the RF oscillator 24 frequency to the reference frequency 20. The phase noise performance of the free running oscillator is worse than the reference crystal oscillator input 20; so the design objective is to set the loop bandwidth as wide as possible to track out as much close in phase noise as possible. Further out phase noise, outside the loop bandwidth, is limited by

20   the oscillator phase noise characteristic. However, there is a compromise well understood by people skilled in the art. This compromise results from the fact that smaller frequency step size (higher resolution) requires division to a lower common phase detector frequency. A PLL with lower loop bandwidth thus has to be used

which consequently degrades the phase noise.

Figure 3 shows a typical implementation of the third method. The reference input 30, starts a pulse traveling down a voltage controlled delay line (VCDL) 32. The pulse is returned to the input 31 and travels down the delay line again. In this way the number of pulses required to match the desired frequency multiplication are produced. The last pulse from the output 35 is phase locked to the next input reference 30 pulse using the phase detector 33 and the loop filter 34. This method suffers from limitations to the PLL implementation. It also faces additional problems with frequency agility as well as the jitter introduced by the delay lock loop because of mismatched delays.

Figure 4 shows the basic concept of the fourth method mentioned above which is known as direct digital synthesis (DDS). As shown in the figure, the clock reference input 40 is sent to a phase accumulator 41. The required phase shift is realized by using a phase to amplitude converter 42 Read only Memory (ROM) look up table. A Digital to Analog Converter (DAC) 43 is used to reconstruct the signal. External filtering 44 is used to filter off the clock and aliasing components from the DAC output thereby resulting in the desired RF signal 45. This method results in very fine frequency resolution, but produces undesired spurious signals and the output signal frequency is limited by the speed of the DAC. The signal frequency for the DDS is limited to Nyquist frequency which is half of the clock frequency to the DAC. Output signal level drops as the Nyquist frequency is approached.

Figure 5 shows a block diagram of one embodiment of the invention.

This arrangement synthesizes a desired lower frequency with high resolution from a fixed frequency high speed reference clock. This is accomplished fully digitally in an ASIC without the use of a VCO, loop filter, or DAC. The high speed reference clock 103 is typically an external input with high frequency absolute accuracy and very low

5 phase noise. Examples of sources are well known in the art and include high frequency crystal oscillators, SAW oscillators, and crystal oscillators with harmonic multiplication. As shown in Figure 5, an edge of the reference clock is delayed by an amount that is controlled by the Accumulator 102 along with a lookup table and programmable delay 106. The edge could be either the rising or falling edge of the

10 reference clock. Separate circuits are used for the control of rising and falling edges of the output signal 108 from the same input edge of the reference clock. This ensures that even if the duty cycle of the input reference is not 50%, the output 108 duty cycle can be controlled as both the rising edge and falling edge delay is triggered from the same edge of the reference clock 103. The desired output duty

15 cycle is typically 50% to maximize the RF power in the fundamental frequency. However, any desired duty cycle of the output signal can be produced for special applications. The output signal 110 frequency is selected by setting the increment value. Typically, the two increment values 101a and 101b are set to be the same. The required increment value 101 is computed by using the following equation:

20 Increment Value = $((f_{ref} / f_{out}) - 1) * 2^n$

where f_{ref} = Reference clock 103 frequency

f_{out} = Output 110 frequency

n = Number of bits in the accumulator math.

Table 1 shows sample calculations for an example where the high speed reference clock 103 is 1000 MHz, and the desired output RF frequency is 734.313739 MHz and n = 12. Using these numbers in the frequency setting equation yields an increment value 101 of 1482. This increment value is added each high

5   speed reference clock 103 cycle to the accumulator to produce a new accumulator value.

The second equation controls the duty cycle of the output. As shown in Figure 5, there are separate blocks to control the rising edge delay (a) and the falling edge delay (b). To accomplish a fixed duty cycle, the increment values 101a

10   and 101b must be the same and the initial start up values 111a and 111b in the accumulator must be set to provide for the desired fixed delay between them. The equation for the initializing value 111b assuming the initializing value for 111a to be zero is as follows:

Initializing Value (111b assuming 111a is 0) $= (f_{ref} / f_{out}) * 2^n * (p/100)$

15   where f_{ref} = Reference clock (103) frequency

f_{out} = Output (110) frequency

n = Number of bits in the accumulator math

p = Percentage duty cycle

For the example shown in Table 1, for duty cycle p = 50 %, the

20   initializing value 111b is calculated to be 2789. Table 1 illustrates that the adder/accumulator 102a starts at 0 and increments 1482 at every rising edge of the reference clock. At the same time adder/accumulator 102b starts at 2789 and increments 1482 every rising edge of the reference edge. When the

adder/accumulator 102 overflows and produces a carry out due to the math addition, an input pulse edge must be ignored or "swallowed". This corresponds to phase wraparound, i.e. the phase shift has reached 360 degrees and must be set to 0 degrees. In the present invention, $2^{\wedge n}$ is calibrated to equal 360 degrees of the

5   reference clock input 103. This calibration is performed in the LUT 105 by a simple mapping of input control bits to desired control lines. The filling of the LUT 105 to perform this requirement would be well understood by those skilled in the art. The LUTs 105 can be implemented using a read only memory or with a microprocessor. The adder/accumulator overflows due to an addition indicates a greater than 360

10   degree delay requirement. This delay is implemented by using the next clock edge rather than delaying from the original clock edge. This allows the programmable delay line 106 to act as a delay line with endless delay capability. For example if the accumulator is using 12 bit math then 360 degrees is equal to $2^{\wedge 12}$ or 4096. In the example shown in Table 1, the accumulator overflows to 4446, which means the

15   overflow bits are set to a value of 1 and accumulator value goes to 4446 – 4096 = 350. The circuit implements the requirement for this value of phase delay in two parts. It activates the pulse swallow circuit 104 to ignore one clock edge, and sets the programmable delay to 350 which completes the rest of the delay requirement. This unique feature of the present invention means that any quantity of overflow bits

20   could be handled. If the addition of the increment value 101 to the accumulator value 102 causes, for example, two overflow bits, then the pulse swallow circuit 104 would ignore or "swallow" 2 pulses. In this way it is possible to synthesis very low frequencies 108 from the high speed clock reference 103. The delay required to

achieve this is limited to one cycle at the high speed reference clock rate. Furthermore, the accuracy of the timing and jitter is excellent, as the time is always relative to the closest edge of the high speed clock reference 103. The output signal phase noise is not controlled by the loop bandwidth nor the phase noise

5   characteristics of the voltage controlled oscillators applied in traditional methods. Instead, the phase noise performance is directly linked to the high speed reference. This reduces both the jitter and phase noise of the synthesized RF output 108. The delayed edge from the programmable delay 106a sets the output RF high 108 by enabling a set-reset flipflop 107. When the delayed edge from the programmable

10   delay 106b reaches the flipflop, it resets the flip flop 107 and causes the RF output 108 to go low. This completes the synthesis of the RF output 108 at the preferred 50% duty cycle rate.

Figure 6 illustrates time plots for the example in Table 1. The upper plot is the high speed reference clock plotted over 5500 degrees. The lower plot is

15   the RF output 108, plotted over that same 5500 degrees of phase shift with respect to the reference clock. The lower plot demonstrated the synthesis of a lower frequency from the high speed reference clock. Optionally the output 108 can be amplified and or filtered to produce a signal that is higher in amplitude and/or having less harmonics.

20   The frequency step size of this invention depends on the frequency and the number of bits n in the accumulator math. It is coarser at frequencies closer to the reference clock frequency, and finer at lower frequency outputs. The worst case step size is the reference frequency divided by 2^n , where n is equal to the

number of bits in the accumulator math. In the example of Table 1, the step size is 1000 MHz divided by 2^n. This gives a step size of approximately 244 KHz. To improve the frequency resolution an increased number of bits in the math can be used. For example with 16 bit math, the frequency resolution improves to

5 approximately 15.2 KHz. Increasing n to 32 bits would result in approximately 0.2Hz frequency resolution. It is only necessary to increase the number of bits of resolution in the adder/accumulators 102, and not necessarily the LUTs 105 and the programmable dividers 106. In essence the number of bits of math used in the adder should be equal to or exceed the number of bits of control in the lookup table

10 and/or programmable delay. The remaining least significant bits can be truncated before the LUTs 105 with negligible effect on the RF output 108 phase noise quality. This means that very fine frequency resolution is achieved with negligible degradation in the phase noise. It can also be seen that the increment values 101 can be changed to provide an essentially instantaneous frequency change. Another

15 aspect of the invention is that the output frequency 108 synthesis range is very wide. The pulse swallow 104 circuit can block multiple reference clock pulses extending the programmable delay indefinitely. The limitation comes from the number of overflow bits allowed in the accumulator. The output frequency range coverage can be DC up to the high speed reference clock frequency. It is desirable to have as

20 high a reference clock frequency as possible for. A higher reference clock frequency extends the useful frequency range and improves the frequency resolution. The upper reference frequency limit of the design is mostly limited by the design speeds of the high speed adders/accumulator 102 and look up tables 105. It understood in

the art that speeds can be increased by parallel processing and other design techniques. For example, multiple high speed adders/accumulator, LUTs or programmable delay lines could be used in parallel to increase the speed and thereby the output frequency capability of the invention. The invention also

5 accommodates plurality of design blocks such as adders, accumulators, pulses swallow circuits, lookup tables, and programmable delay lines.

In an alternative arrangement of the invention it is also possible to implement the invention on every 180 degrees of the reference clock using both the rising and the falling edges. Another alternative arrangement is to position the clock

10 swallow circuit following the programmable delay line.

. In an alternative arrangement of the invention it is also possible to remove the adder/accumulators 102 and replace the LUT 105 with a larger LUT 105. A simple counter could increment the values in the LUT 105. The LUT 105 would in this case hold the pre-added values, and just cycle through them until the pattern

15 repeats.

In an alternative arrangement of the invention it is also possible to compromise latency for the speed of the device. It does not matter how many clock cycles it takes to implement an adder or LUT for example, as long as we get valid data out every reference clock cycle.

20 It is possible to use a selection of different lookup tables 105 or offset values to compensate for the temperature effect on the programmable delay lines 106. It is also possible to vary the implementation of the delay lines by altering the input clock signal. Examples of clock alteration would include frequency

multiplication, division, or phase shifting.